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NASA's new vacuum-channel nanoelectronics rely on Park Systems AFM

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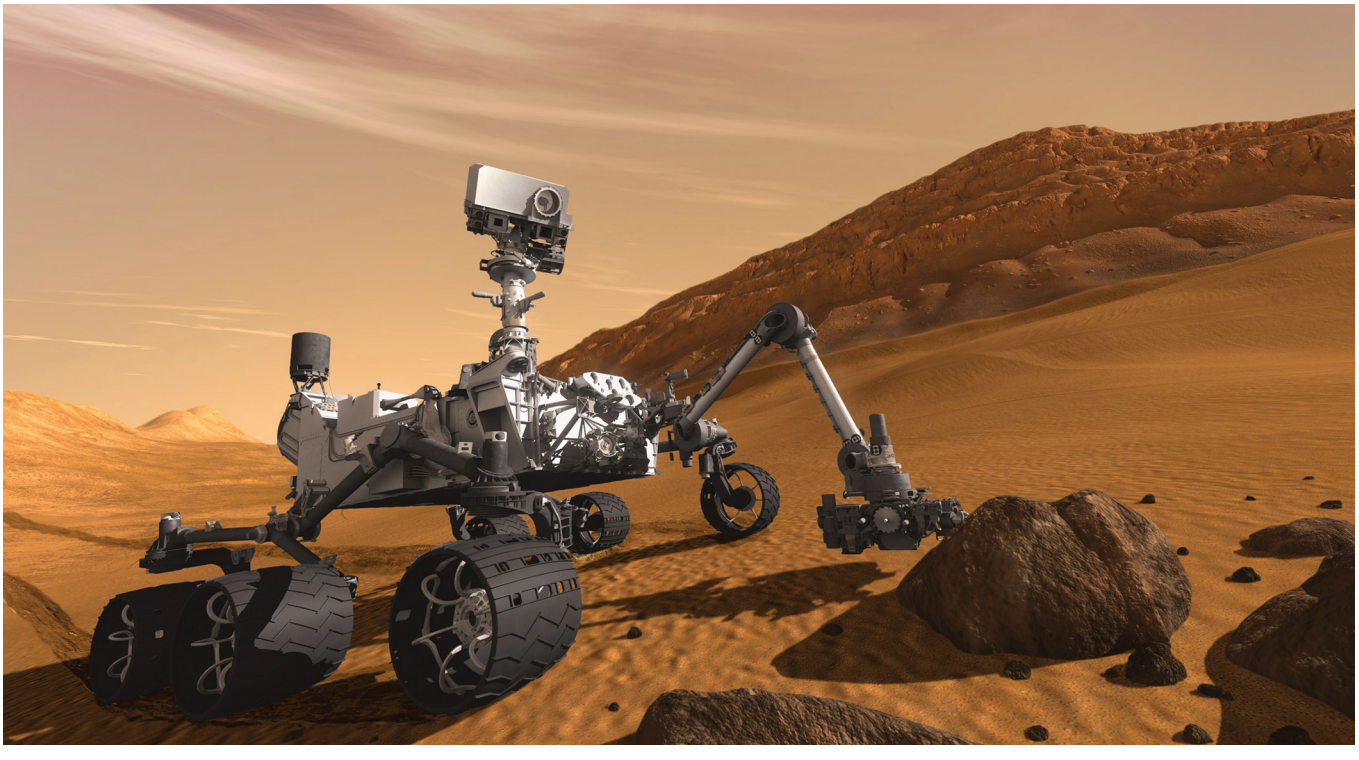
Using scanning capacitance microscopy with a Park Systems atomic force microscope a team at NASA successfully characterized both the spatial variations in capacitance as well as the topography of vacuum-channel nanoelectronic transistors.

Imagine the not-too-distant future when a NASA spacecraft edges silently into orbit around Mars. Its 473-million-mile journey included a trip around the sun to sling shot itself into in geosynchronous orbit. Its mission: gather new site-specific details and deploy a rover as preludes to the first human mission to the red planet. But before anyone can take 'one giant leap', the Mars Path Marker needs to supply fresh data to anxious scientists back on earth.

The probe cost $1.8 billion. Its planning, construction and flight time to Mars took eight years and thousands of work hours from all across the aerospace supply chain.

Red lights are now flashing all across screens back on earth at NASA's Jet Propulsion Laboratory in Pasadena, California. The probe remains inactive while its earth-side controllers grow frantic. Path Marker should have automatically powered-up for its first mapping transit, but instead hangs quietly above the ruddy Martian landscape.



Unbeknownst to controllers on earth, Path Marker wasn't responding because of a short-circuit 'latch-up' in its silicon processors. Communications won't resume for now—maybe not ever.

Earth could not see it happen, but when Path Marker flew around Sol, its passage coincided with an unusually large solar flare on the backside of oursun. More energy than what usually strikes Mars in six months was released in a series of coronal explosions, sending cascades of lethal, heavy ions plowing through Path Marker's delicate solid-state transistors as if its shielding wasn't even there.

Despite the best of plans, precautions and preparations, thisspacecraftis stuck in perpetual 'neutral.' Mission specialistsare trying all availablemission-saving workarounds, but only time will tell.

NASA researcher Dr. Jin-Woo Han hopes to prevent a critical failure in an important mission like this fictional account of the Mars Path Marker. In reality NASA has experienced all types of solid-state electronic failures during its decades of manned and robotic explorations. In his work, Dr. Han documented nine different types of failures in 17 named missions as well as many more that did not cause a mission failure, but impeded or slowed a program.

Although the Mars Path Marker mission is fictional, the need for a better semiconductor technology for deep space exploration is very real. That need is why Dr. Han and colleagues have placed hope in a new approach to solid state transistors that utilizessome of the same principles that gave vacuum tubes their role in humanity's first electronic products more than 100 years ago.

Han is a scientist at NASA's Ames Research Center for Nanotechnology in Moffett Field, California. The center is led by Dr. Meyya Meyyappan; Dr. Han leads the vacuum device research team within the 20-person organization. One of his most recent research efforts is tied to his theories and practical applications that leverage the advantages of vacuum for creating better electron flow, but without the drawbacks in existing solid-state technology that NASA frequently faces. The new transistors, called vacuum-channel nanoelectronic devices, are not prone to disruption by cosmic radiation, solar flares, radical temperature changes or similar dangers that can be encountered once a spacecraft (or humans) leave earth's magnetic fields and dense atmosphere.

The challenges of space exploration are daunting. While loss of life tops many potentially egregious outcomes, damage to spacecraft instruments occurs much more commonly than the general public may realize. This damage remains a source of concentrated research and engineering efforts to mitigate and remedy problems that can lead to lack-luster performance or full system failures. The efforts to ensure safe and productive operation in satellites, probes and spacecraft is second only to the agency's zeal for keeping human space flight safe.

How can early 20th century vacuum tube technology solve NASA's very 21st century problems? First of all, the vacuum nanotechnology that NASA is developing is generations beyond conventional vacuum tube engineering as it stood in the early 20th century. But vacuum-channel nanostructures and conventional vacuum tubes share essential functional similarities that make Dr. Han's devices ideal candidates to replace today's most robust silicon-based transistors.

Transistors enjoy their role in electronic technology because of their unique abilities to amplify and switch electronic signals as well as electrical power. Power or current applied to one set of terminals controls the current as it flows to another terminal pair (emitters/collectors). And while a practical solid-state transistor was proposed in 1926 by Canadian researchers, materials science only matured enough for production in 1947; the landmark year in which researchers at the AT&T Bell Labs (New Jersey, USA), and independently a year later in France proposed designs that would become the forefathers of today's microelectronic wonders.

Practical vacuum tube components came into play before 1910, and have several important advantages compared to solid-state transistors including their superior electron mobility. Like their solid-state cousins, tube transistors function by moving electrons unidirectionally from the emitter (a cathode) to be collected by the anode across a vacuum. Tubes fell out of favor for most low and medium power applications due to the advantages of solid-state construction including much smaller size and weight, ruggedness that exceeded old-style tubes, their aggregation ability that enabled today's integrated circuits (ICs), and zero warm-up time – silicon transistors requireno cathode warming function. Solid-state devices also provide substantially greater electrical current efficiency.

It's easy to see why solid-state electronics won a place in aerospace engineering. But once we actually got into space, we learned quickly that even robust silicon transistors were no match for deep space radiation. To make the best transistors that we had "good enough" for space, NASA mastered the process of creating backup systems and a

host of other measures to keep missions on track. It alsopartnered with other agencies like DARPA (Defense Advanced Research Projects Agency) and the US Department of Defense to develop alternate technologies such as gallium arsenide (GaAs), gallium nitride (GaN), and the latest work from Dr. Han's nanotech vacuum team. GaAs and GaN are much more robust than silicon, but decades of research have proven them less suitable for construction complex ICs than silicon.

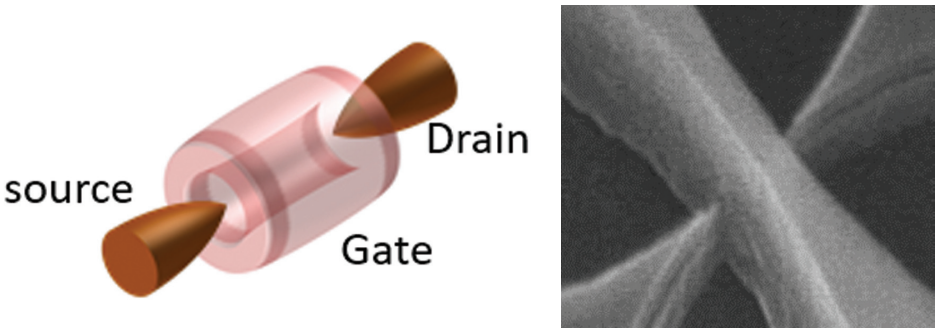


FIGURE 1. The most promising material and design combination is a GAA nanowire in a vacuum gate dielectric.

Although conventional solid-state transistors enjoy clear advantages in terrestrial applications, in-space damage typically comes in three forms: instantaneous, cumulative and catastrophic. While the first two effects can frequently be worked around due to NASA's extensive reliance on back-up systems, catastrophic effects can be "mission enders."

Dealing with likely and possible performance disruptions costs NASA dearly in terms of extra weight, design time to createmultiple backup systems that can also complicate missions whileconsuming valuable payload space. Imagine if using a laptop computer on earth required double or even triple the amount of vital components—that laptop would easily be a third larger and more expensive. For NASA, ignoring risks will impede success or in worst-case situations lead to a disaster that costs millions and could even endanger lives if components weretied to a human spaceflight mission.

A common way to deal with these unknowns is to overbuild—create more circuit pathways or entire redundant subsystems because some components will almost certainly be "sacrificed" during encounters with space radiation. NASA frequently must opt for "acceptable" performance instead of what might ideally be possible simply because they cannot count of systems that have optimal performance will remain that way throughout an entire mission.

The advantage a controlled vacuum has in transistors is tied to the fact that solid-state devices can experience long-term failures resulting from additive and cumulative effects from multiple bombardments of ionizing radiation that destroys device features at nanometer scale. This most commonly occurs when the total ionizing dose causes gradual parametric shifts, resulting in on-state current reductions and an increase in off-stage current leakage. A vacuum-based device does not typically suffer from these same effects in part because the absence of material (gases or solids) in the space between emitters and collectors not only speeds the flow of electrons but in essence is protective because there is very little present in this tiny void that might be damaged by ionizing radiation.

Dr. Han's team studied several different compounds and structures that could be utilized to construct the vacuum channel nano devices that would eventually prove likely successors to conventional transistors. These materials included bulk MOS, silicon-on-insulator (SOI), gate-all-around (GAA) MOSFET and what proved to be the most promising material and design combination, a GAA nanowire in a vacuum gate dielectric (**FIGURE 1**).

To be effective and meet NASA's requirements, new transistor technology had to be manufacturable at industrial scale using existing processes and techniques common to conventional silicon fabs or similar infrastructure. The ideal design would bring the "best of both worlds" together for a solution that is electrically sound, practical and compact as well as lightweight and reliable in the face of exposure to radiation and radical temperature fluctuations.

"But we did not ever approach this as a replacement for all silicon electronics or silicon transistors at large," said Dr. Han. "While the devices could easily be used on earth—that is where we tested them in gamma radiation chambers after all—but the cost efficiencies of regular silicon MOSFET could not very likely improved by our vacuum-channel nanoelectronic designs."

To measure device performance Dr. Han and his team employed a Scanning Capacitance Microscope (SCM) with an Atomic Force Microscope (AFM) from Park Systems.

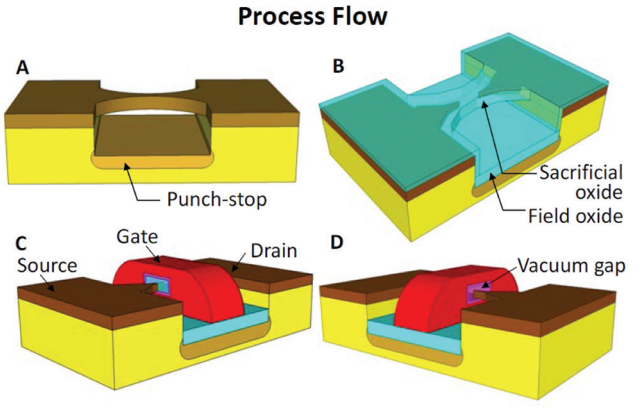


FIGURE 2. New transistor technology had to be manufacturable at industrial scale using existing processes and techniques.

They investigated the nanoscale properties of vacuum-channel devices, seeking to ascertain their viability as a transistor while also observing if fabrication methodology for gate insulators can be controlled.

"SCM with AFM is a powerful combination for investigating transistor devices—together, the two methods provide the user with a non-destructive process of characterizing both charge distribution and surface topography with high spatial resolution and sensitivity," said Byong Kim, Analytical Systems Director, Park Systems.

Kim explained that atomic force microscopy with SCM is ideal for investigating transistor designs at the nano scale. Together, the two methods provide researchers with non-destructive processes for characterizing both charge distribution and surface topography with high spatial resolution and sensitivity. In SCM, a metal probe tip and a highly sensitive capacitance sensor augment standard AFM hardware. During testing, voltage is applied between the probe tip and the sample surface. This creates a pair of capacitors in series (when examining metal-oxide-semiconductor devices) from the insulating oxide layer on the device surface and the active depletion layer at the interfacial region located between the oxide layer and doped silicon. Total capacitance is then determined by the thicknesses of the oxide layer as well as the depletion layer, which is influenced by the level of silicon substrate dopingas well as the amount of DC voltage being applied between the tip and device's surface.

Dr. Han reported that by utilizing scanning capacitance microscopy with a Park Systems atomic force microscope the team successfully characterized both the spatial variations in capacitance as well as the topography of his vacuum-channel nanoelectronic transistors.

By examining the line profiles of the topography and capacitance data acquired down an identical path along the device's source-drain interface, further insight was gained into the relationship between key physical structures and recorded changes in capacitance.

The nanoelectronic device's topography (at the source-drain interface) was imaged and revealed a vacuum-channel spanning 250 nm in length with peaks and valleys separated by a distance of approximately 5 nm (**FIGURES 3-5**). The electrical functionality of the device was assessed through the acquisition of a capacitance map. This map revealed a relatively negatively charged (-1.4 to -1.8μV) source-drain terminal and adjacent quantum dot followed by a relatively positively charged vacuum-channel (2μV) and another dot-terminal structure (-1.4 to -1.8μV) on the other end of the source-drain interface. This alternating series of capacitance changes at key structural points suggest that the device is fully capable of functioning as an effective transistor.

NASA is now working towards next steps to investigate the potential of producing vacuum-channel nanoelectronic devices in higher volumes for further study. The team utilized standard semiconductor manufacturing techniques, so while fabrication is within existing process and materials technologies, settling on the ideal material for the transistors is also still being investigated.

"While the work initially focused on silicon as an underlying technology, we next want to explore silicon carbide and graphene as alternatives—technologies that are more robust. Also, the charge emission efficiency of silicon may not be sufficient and we saw some degradation due to oxidization," he remarked. "While we have demonstrated

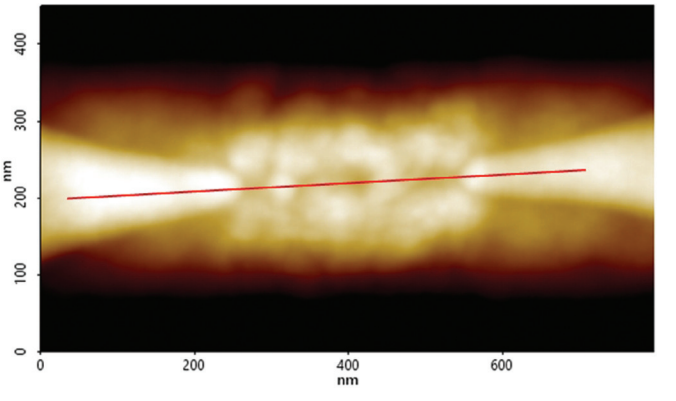


FIGURE 3. Contact mode AFM topography image of the vacuum-channel device's source-drain interface. The overlaid red line corresponds to the topography line profile displayed in Figure 4. Scan size: 450 x 800 nm.

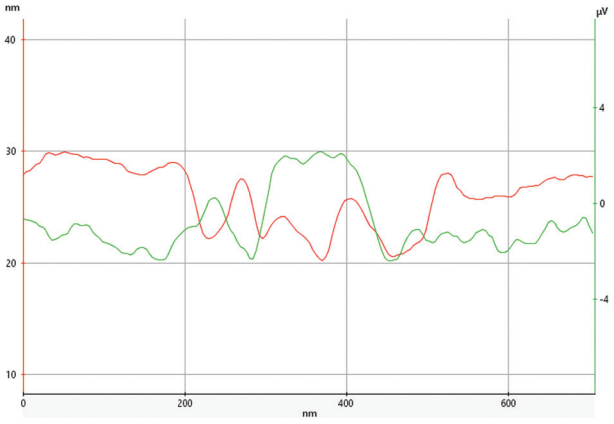


FIGURE 4. Line profiles of the AFM topography (red, left y-axis in nm) and the capacitance data (green, right y-axis in μV) of the device area scanned in Figures 3 and 5.

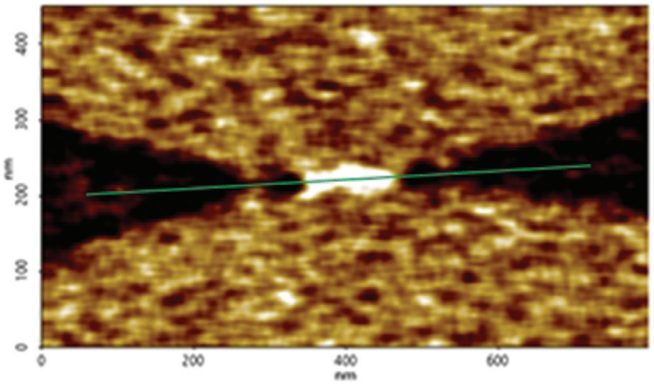


FIGURE 5. An SCM capacitance image of the region containing the device's source-drain in-terface. Brighter colors correspond to relatively more positively charged areas on the device whereas darker colors correspond to relatively more negatively charged areas. The overlaid green line corresponds to the capacitance line profile displayed in Figure 4. Scan size: 450 x 800 nm.

that a silicon vacuum-channel nanoelectronic device is possible. We now need to look at better emitter efficiency and reliability, balanced against ease of manufacturing – everything is a tradeoff in some regards."

The Ames Research Center is open to partnering through industrial and university collaboration, like the work it has done in conjunction with Park Systems. NASA is already working with additional industrial partners and welcomes further collaboration. ◆